



Fig. 1a

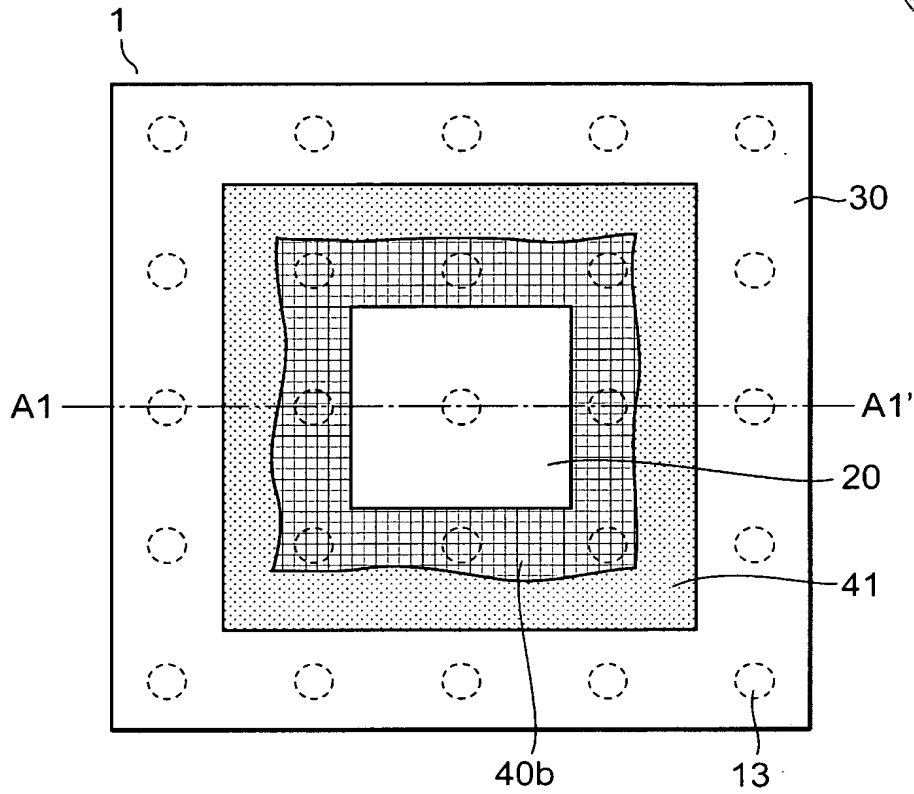
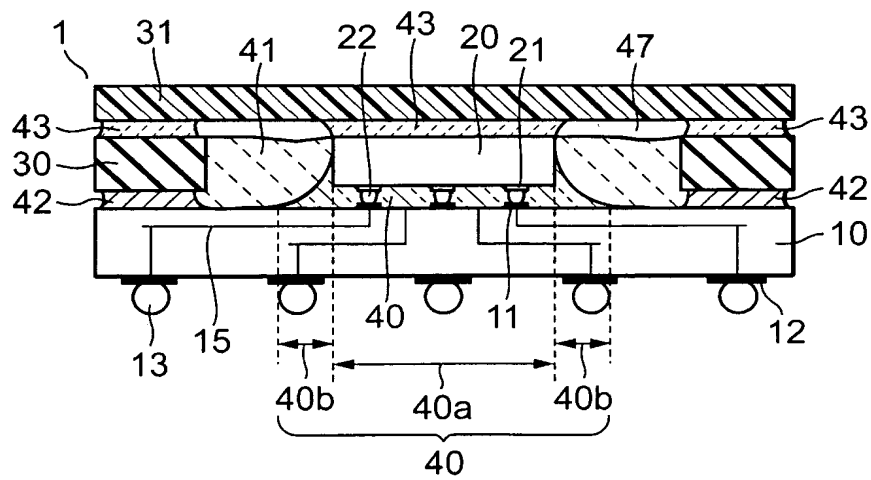


Fig. 1b



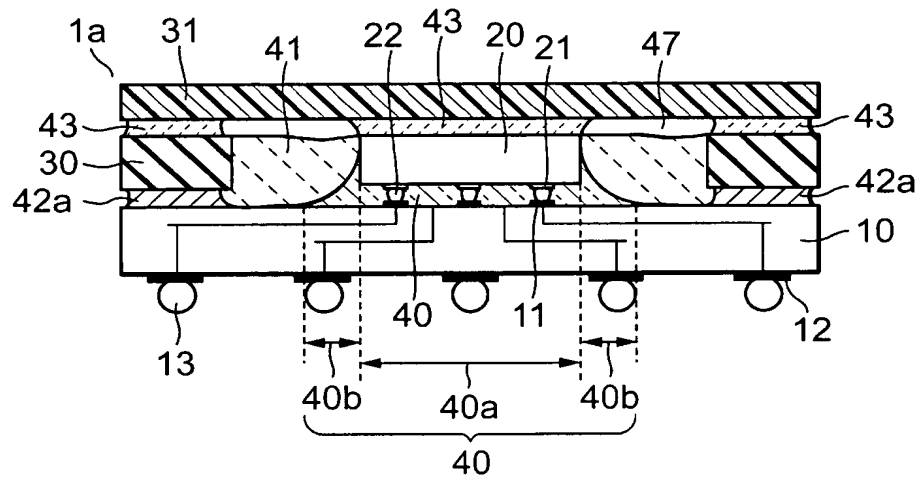


Fig. 3a

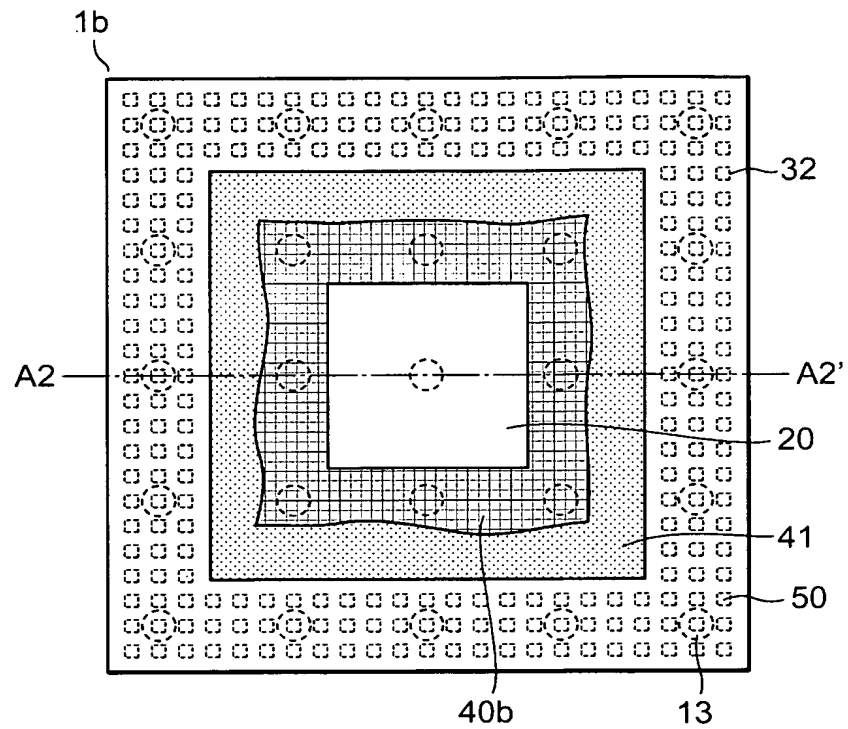


Fig. 3b

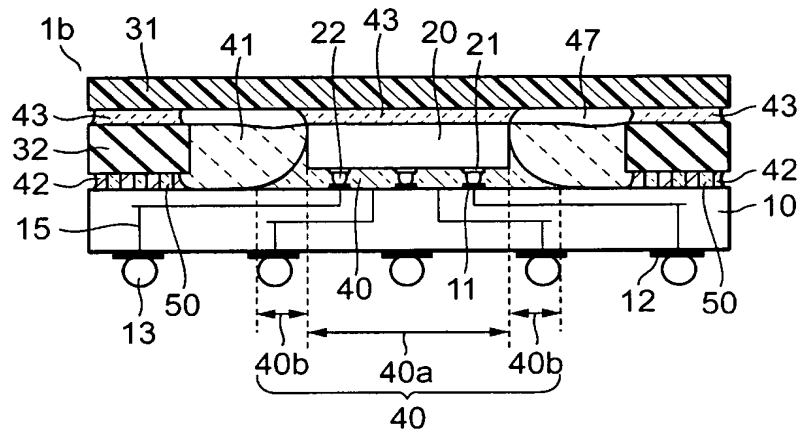


Fig. 3c

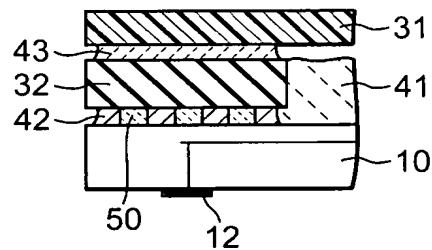
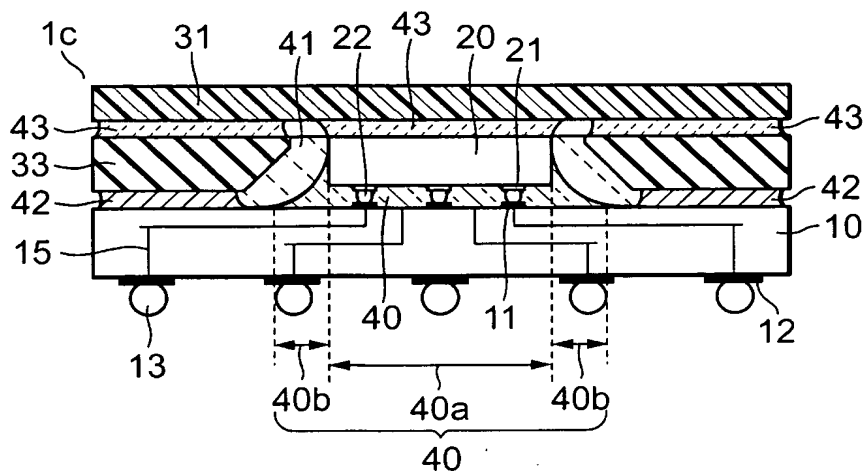


Fig. 4



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Fig. 5a

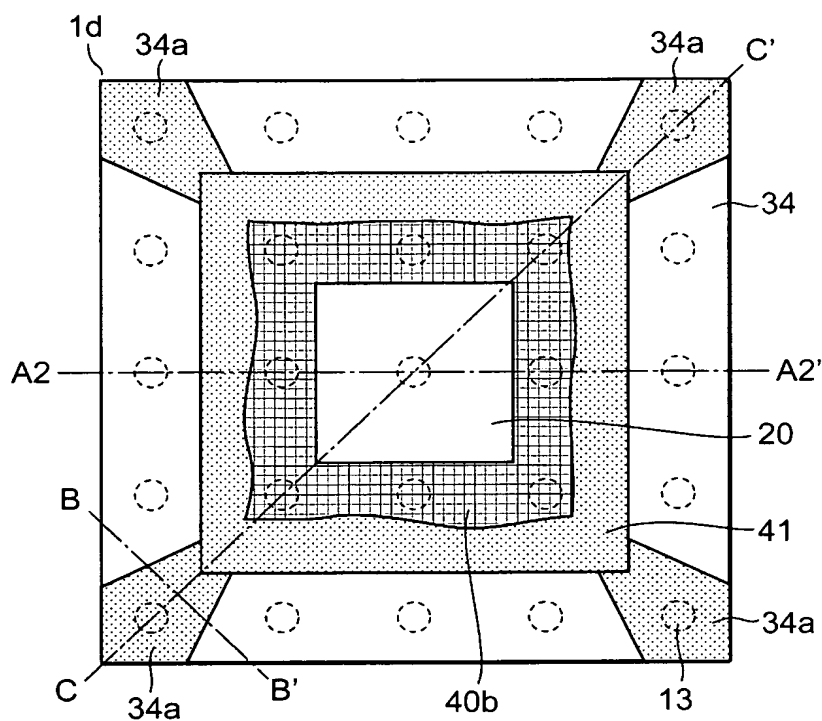


Fig. 5b

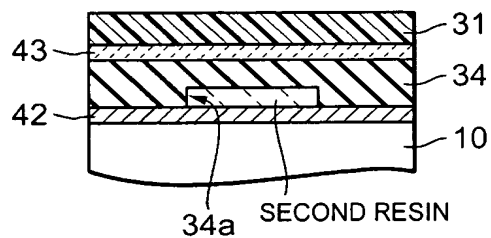


Fig. 5c

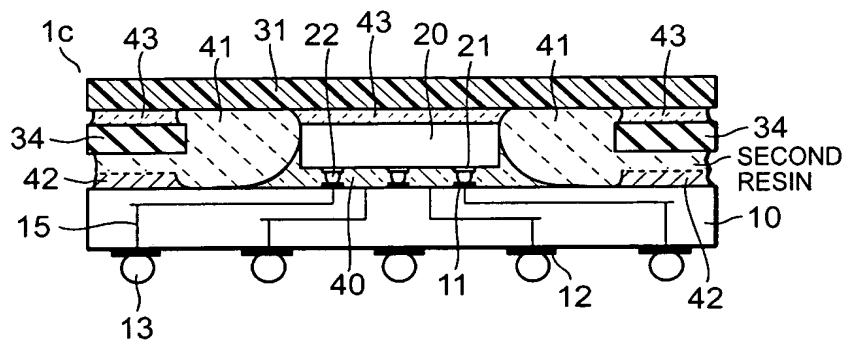


Fig. 6

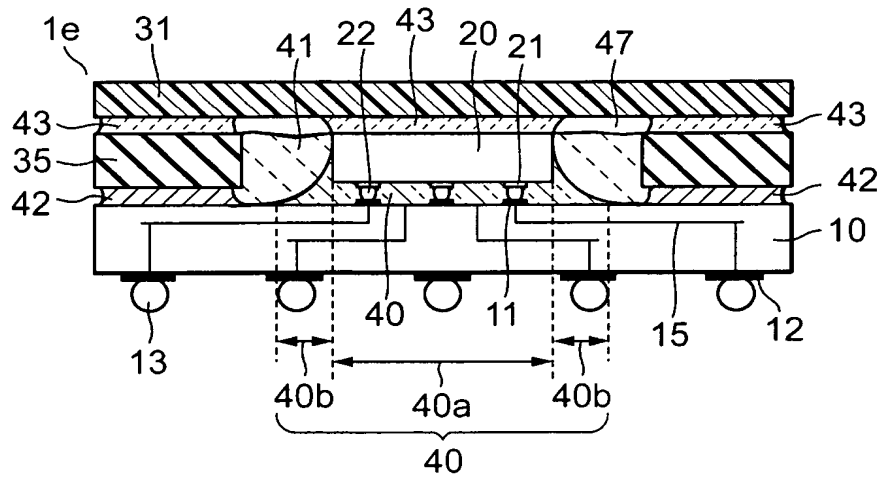
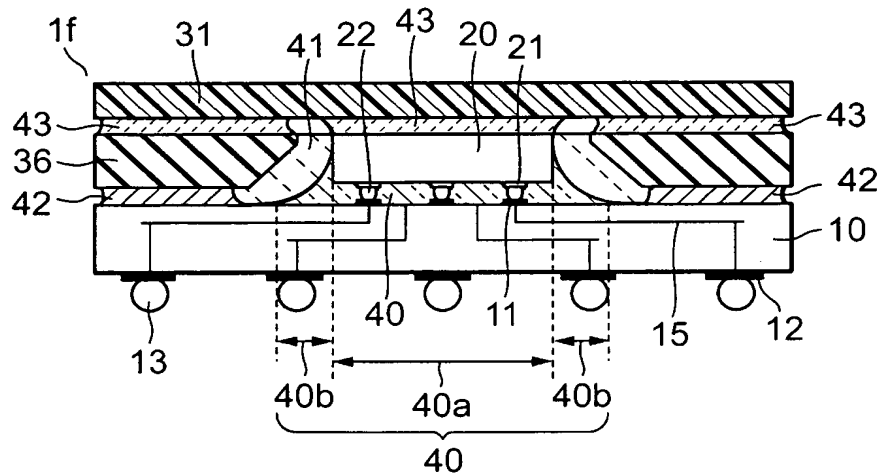


Fig. 7

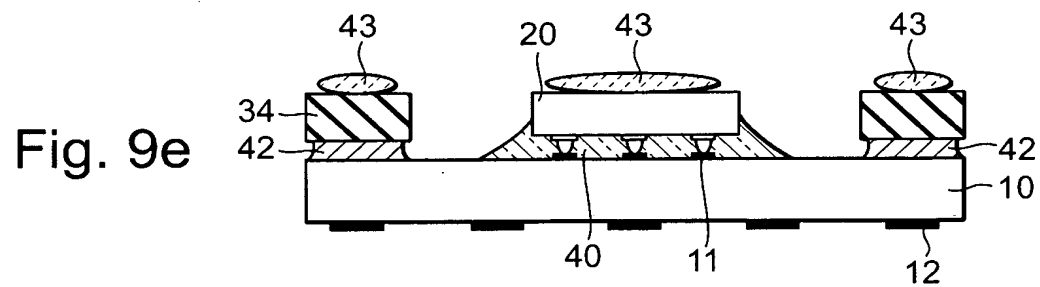
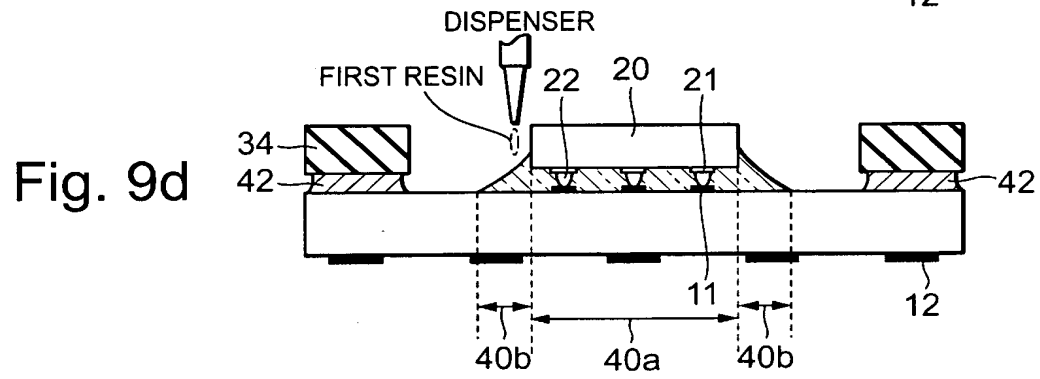
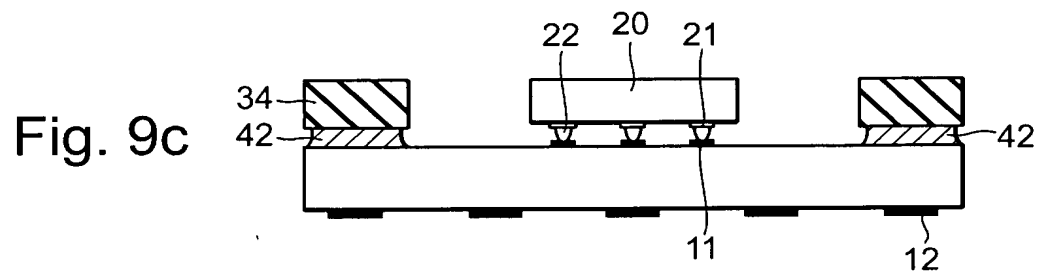
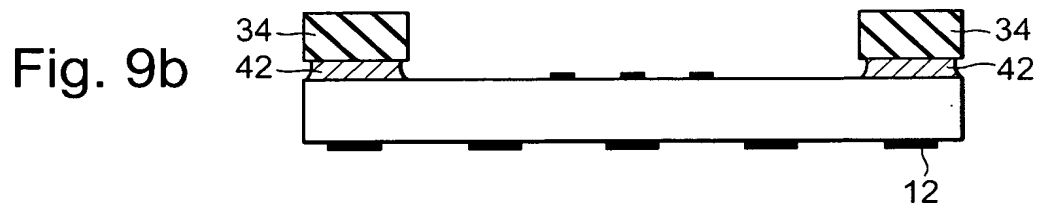
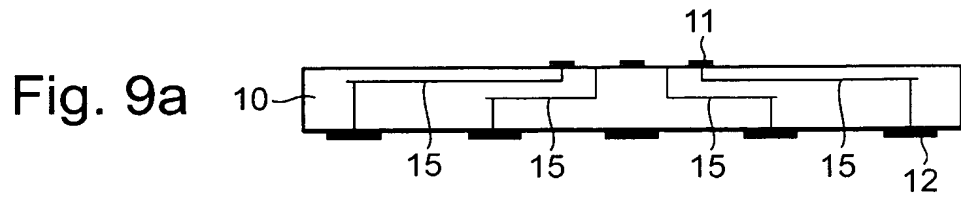


A cross-sectional view of a semiconductor device. It shows a substrate 10 with a top layer 11 and a bottom layer 12. A series of vertical structures 15 are formed between the top and bottom layers.

FIG. 1 is a cross-sectional view of a semiconductor device 10. The device includes a substrate 11 with a central region 40 and side regions 12. A first resin layer 20 is formed on the central region 40, and a second resin layer 21 is formed on the side regions 12. A dispenser 22 is shown dispensing the first resin 20. The central region 40 is divided into three sub-regions: 40a (central) and 40b (side). The side regions 12 are also divided into sub-regions 40b and 40a. The device is mounted on a base 30 via solder bumps 42.

[illegible]

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Fig. 9f

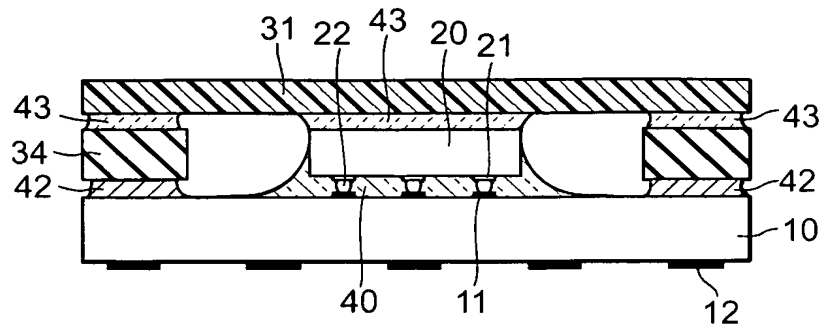


Fig. 9g

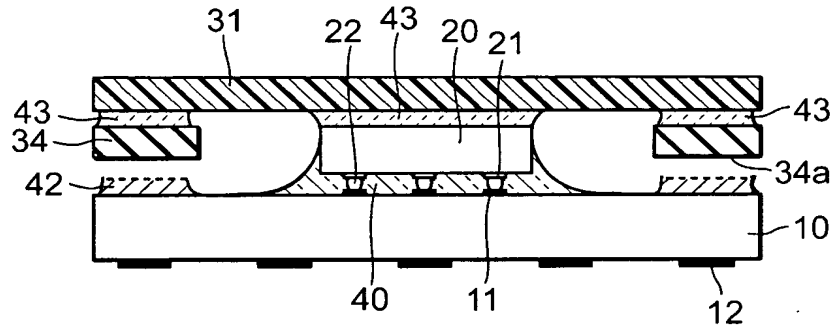


Fig. 9h

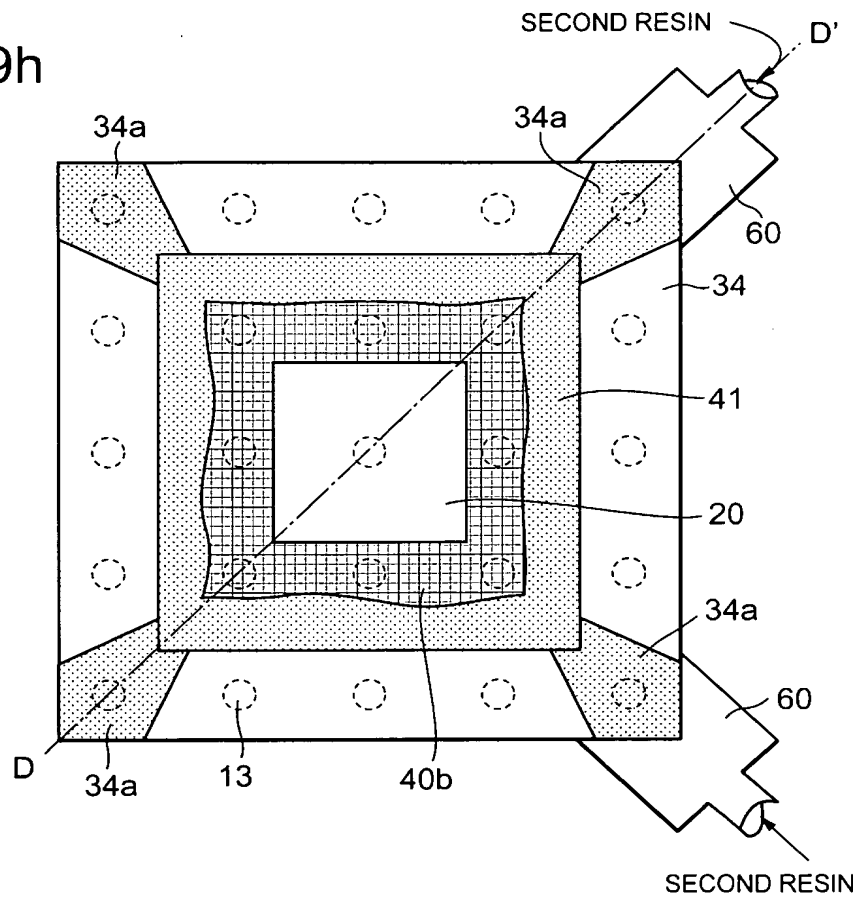


Fig. 9i

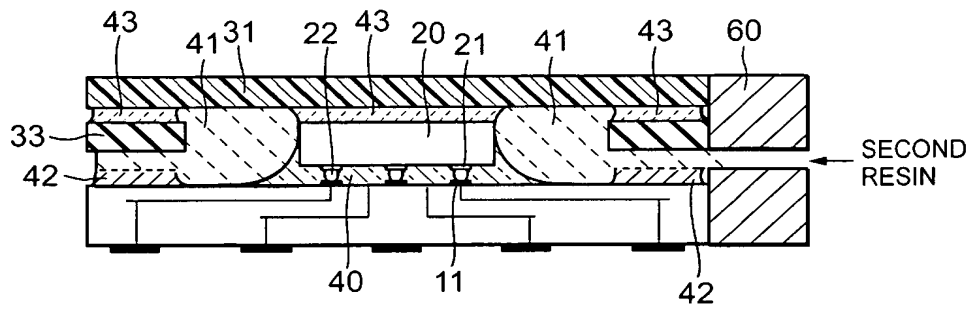


Fig.10a

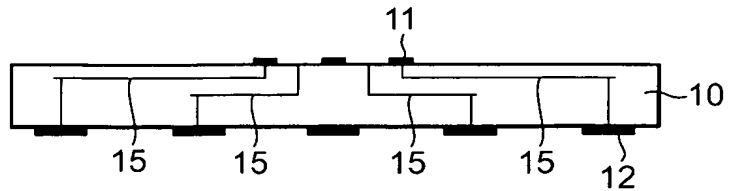


Fig.10b

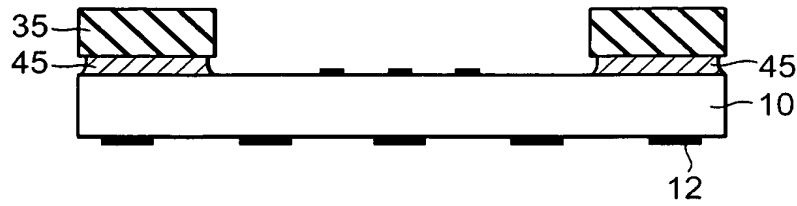


Fig.10c

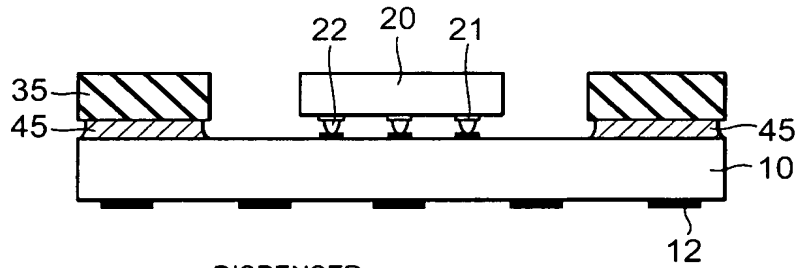


Fig.10d

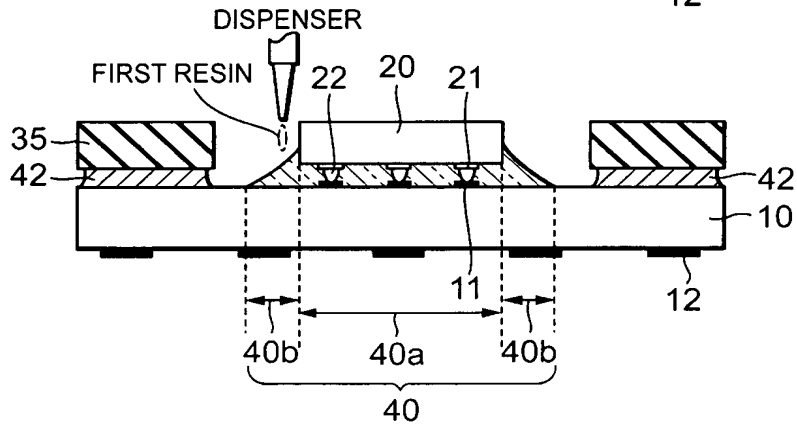
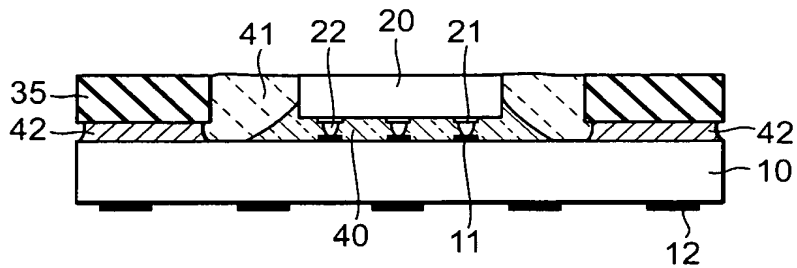


Fig.10e



[illegible]

Fig.11a

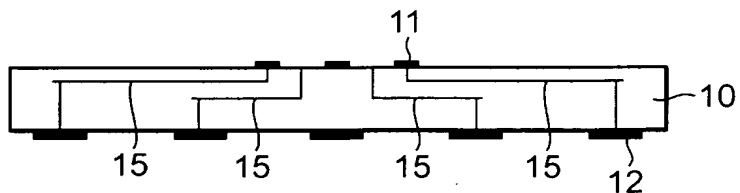


Fig.11b

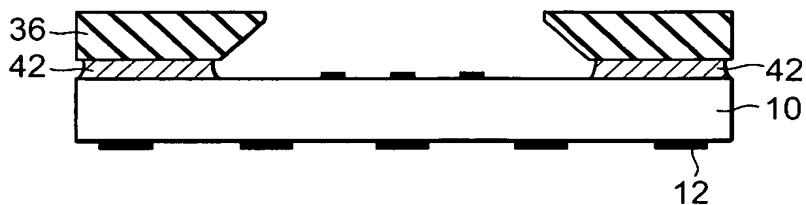


Fig.11c

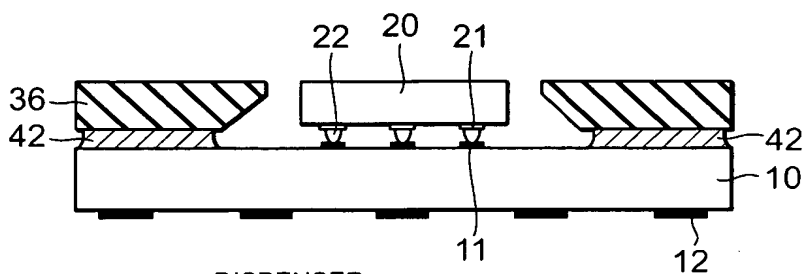


Fig.11d

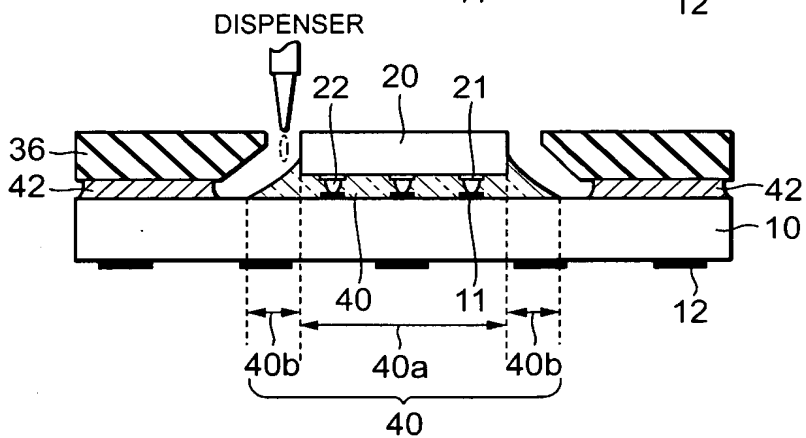


Fig.11e

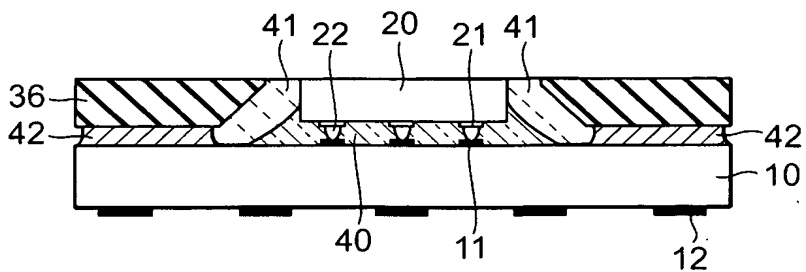


Fig.11f

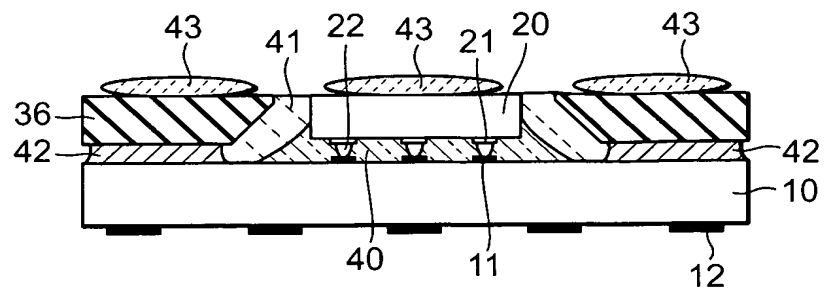


Fig.11g

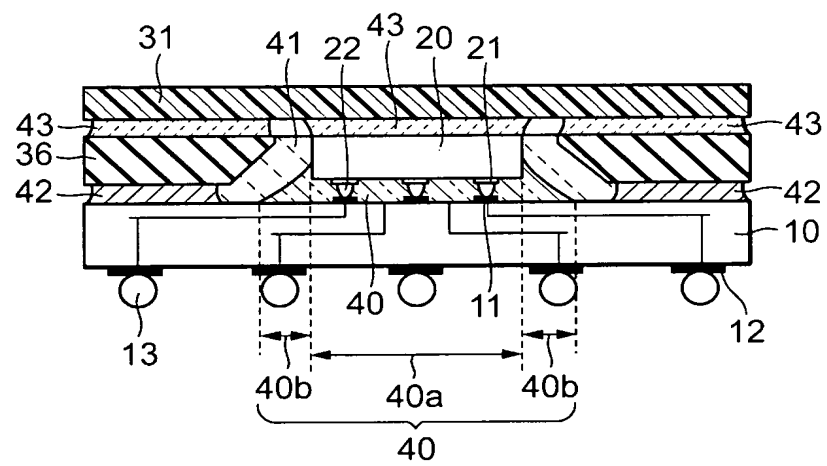


Fig.12a

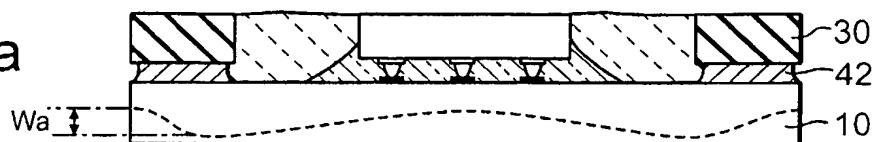


Fig.12b

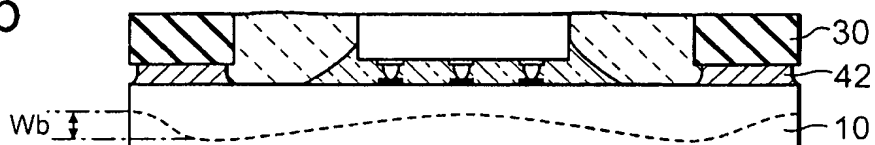


Fig.12c

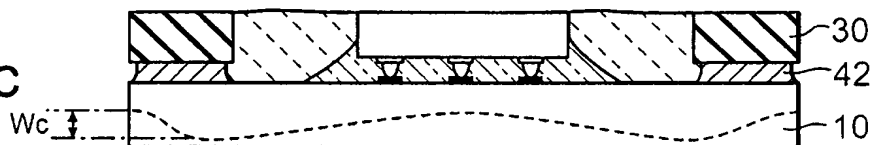


Fig.12d

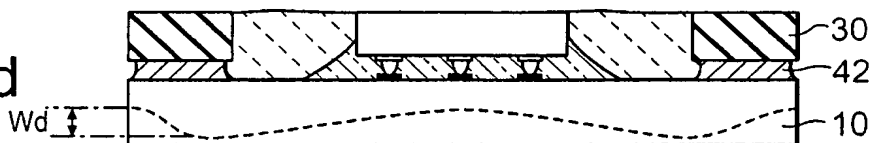


Fig.12e

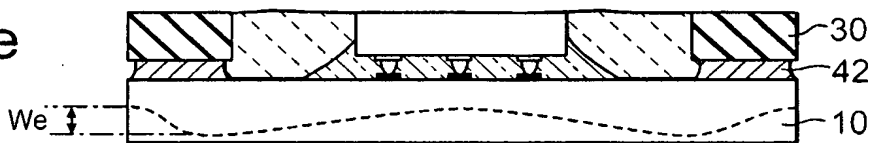
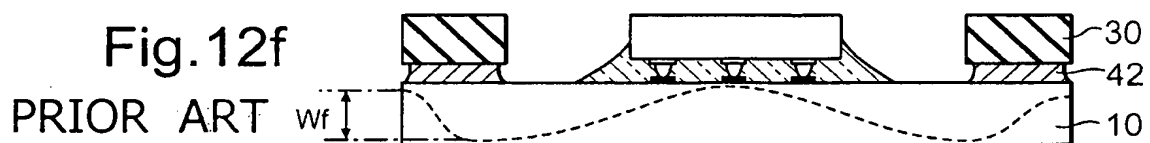


Fig.12f



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Fig.13

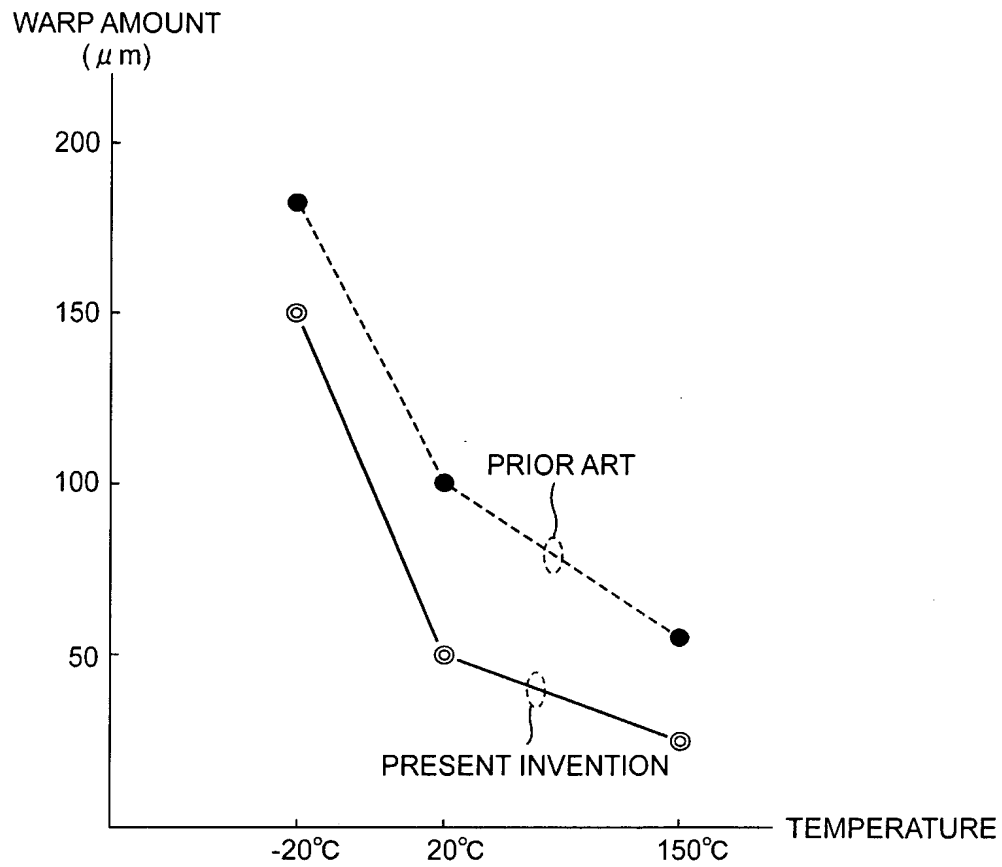


Fig.14a PRIOR ART

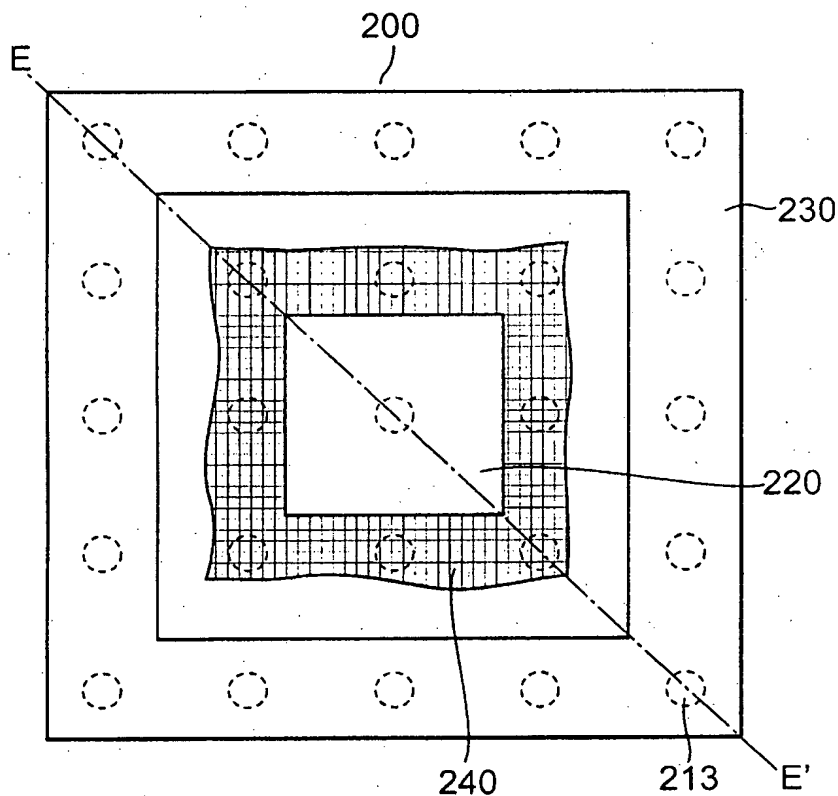
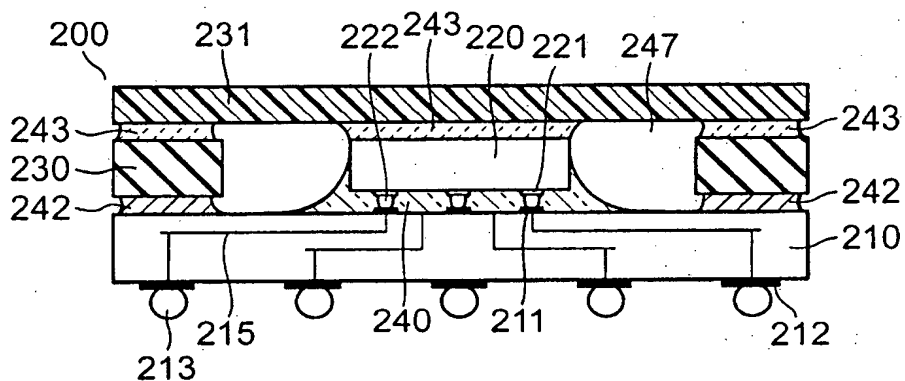


Fig.14b PRIOR ART



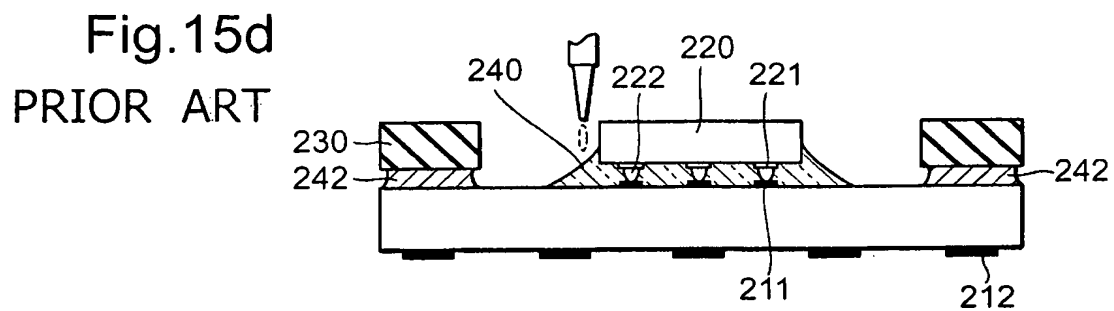
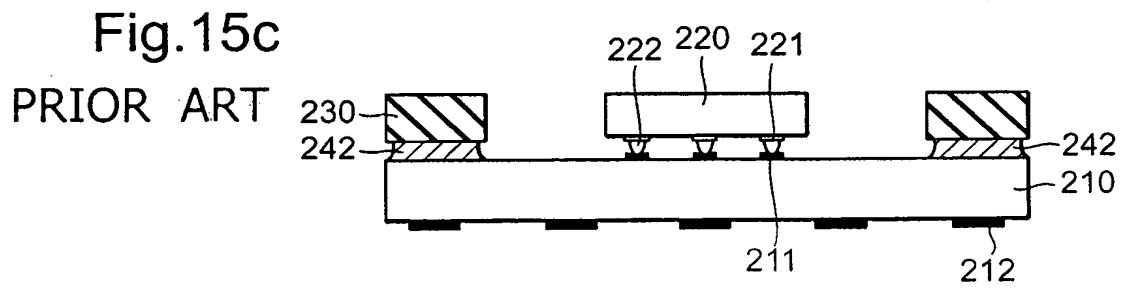
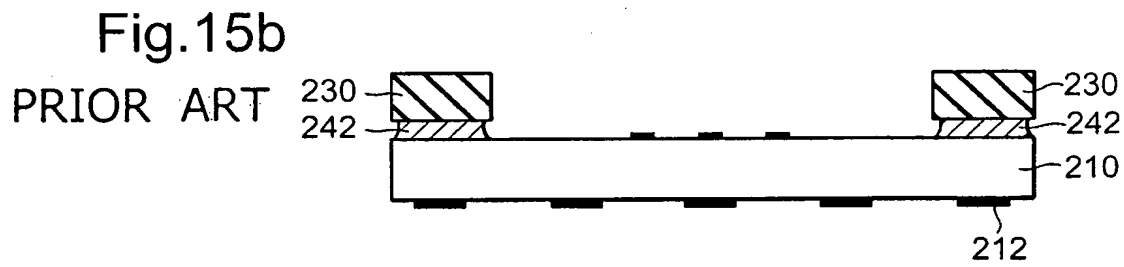
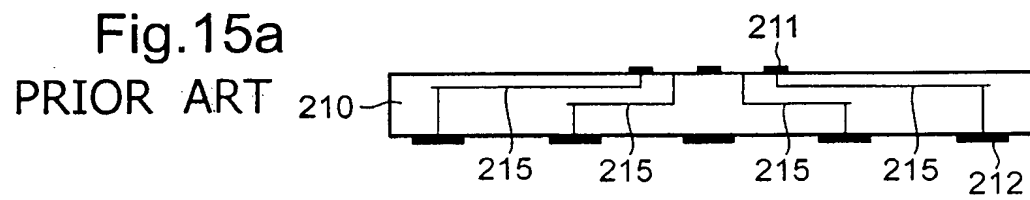


Fig. 15e
PRIOR ART

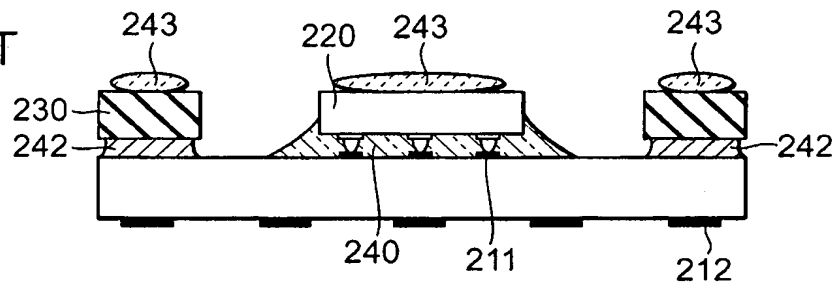


Fig. 15f

PRIOR ART

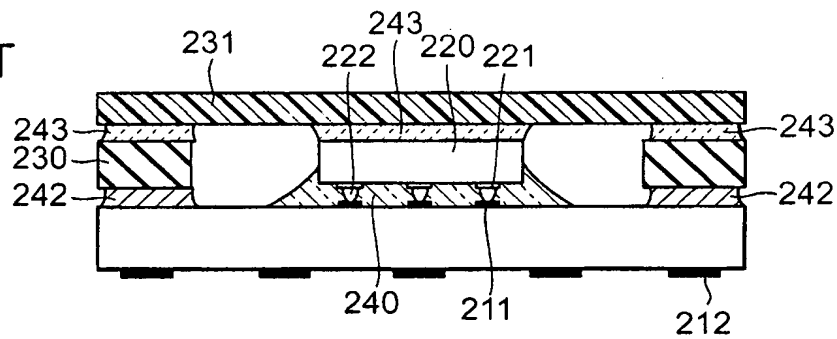


Fig. 15g
PRIOR ART

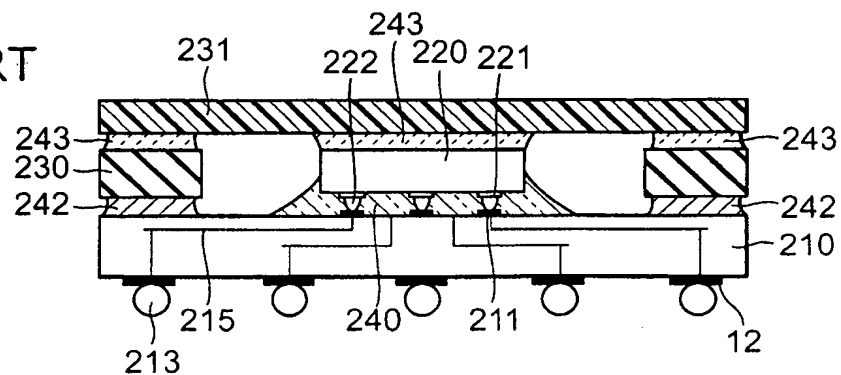
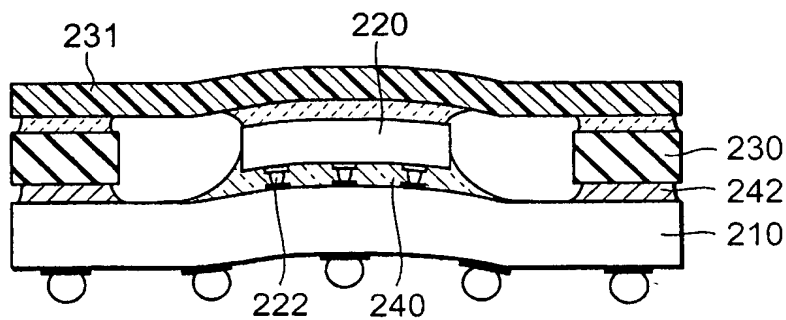
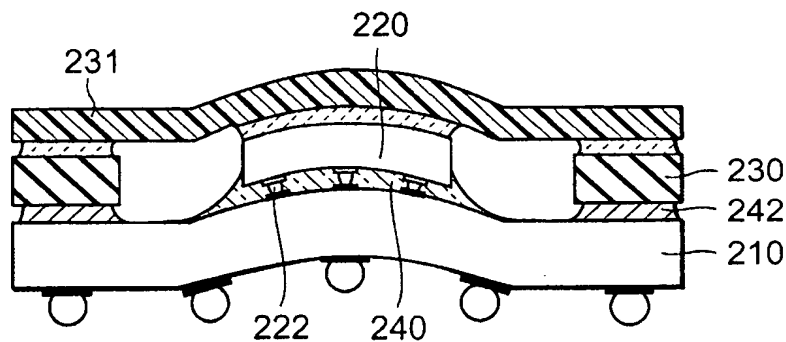


Fig.16a
PRIOR ART



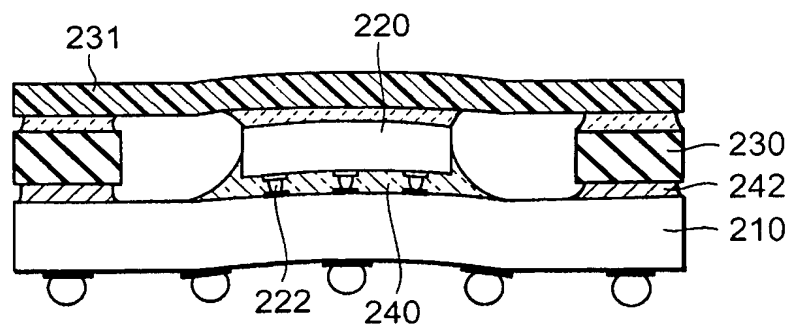
ROOM TEMPERATURE STATE (20°C)

Fig.16b
PRIOR ART



LOW TEMPERATURE STATE (-45°C)

Fig.16c
PRIOR ART



HIGH TEMPERATURE STATE (150°C)

Fig.17 PRIOR ART

